[Total No. of Questions - 9] [Total No. of Printed Pages - 4]
(2125)

15221

B. Tech 6th Semester Examination

Electronics Logic Circuit Design (OS)

EEE-6001

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all, selecting one question each from section A, B, C & D. Section-E is compulsory. Take suitable assumption if required.

SECTION - A

1. A long input sequence enters a one-input one-output synchronous sequential circuit, that is required to produce an output symbol z = 1 whenever the sequence 1111 occurs. Overlapping sequences are accepted; for example, if the input sequence is 01011111 · · ·, the required output sequence is 00000011 · · ·

   (a) Draw a state diagram.

   (b) Select an assignment and show the excitation and output tables.

   (c) Write down the excitation functions for SR flip-flops, and draw the corresponding logic diagram. (20)

2. Design a one-input one-output synchronous sequential circuit that examines the input sequence in nonoverlapping strings having three input symbols each and produces an output symbol 1 that is coincident with the last input symbol of the

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string if and only if the string consisted of either two or three 1's. For example, if the input sequence is 010101110, the required output sequence is 000001001. Use SR flip-flops in your realization. (20)

SECTION - B

3. Determine which of the machines with the following specifications is realizable with a finite number of states. If any machine is not realizable, explain why.

   (a) A machine is to produce an output symbol 1 whenever the number of 1's in the input sequence, starting at t = 1, exceeds the number of 0's. For example, if the input sequence is 01100111, the required output sequence is 00100011.

   (b) A machine with a single input line and 10 output lines numbered 0 through 9 is to be designed such that, following the nth input symbol, only one output symbol 1 will be produced on the line whose corresponding number is equal to the nth digit of π (i.e., 3.14 · · ·) (20)

4. Design a Decade counter. (Use D flip Flops) (20)

SECTION - C

5. An SIC fundamental-mode sequential circuit with two inputs, x_1 and x_2, and two outputs, z_1 and z_2, is to be designed so that z_i (for i = 1, 2) takes on the value 1 if and only if x_i was the input whose value changed last.

   (a) Find a minimum-row reduced flow table.

   (b) Assuming that all inputs are available in an uncomplemented as well as a complemented form, show a realization using NAND gates. (20)

6. At a junction of a single-track railroad and a road, traffic lights are to be installed. The lights are to be controlled by switches that are pressed or released by the trains. When a train approaches the junction from either direction and is within 1500 feet from it, the lights are to change from green to red and remain red until the train is 1500 feet past the junction.

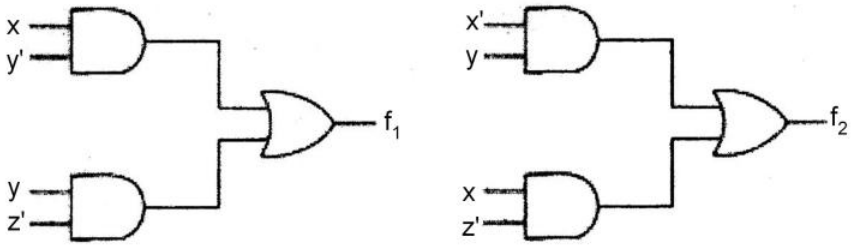
   (a) Write a primitive flow table and reduce it. You may assume that the length of a train is smaller than 3000 feet.

   (b) Show a circuit realization of the light-control network.

   (c) Repeat the design if it is known that the trains may be longer than 3000 feet. (20)

SECTION - D

7. Consider the two-output circuit shown in Figure below. Without inserting any extra gates in it, make both outputs SIC hazard-free. You are allowed to add connections to the circuit. (20)



8. What is decomposition? Also explain conditions for serial and parallel decomposition by taking suitable examples. (20)

SECTION - E

9. (a) Write different steps for the synthesis of Synchronous sequential circuits.

   (b) Draw the circuit of a mod-5 counter.

   (c) Can we convert D flip Flop to JK flip Flop? If yes then How and if no then why not? Justify your answer.

   (d) Draw the circuit of a 3 bit Shift register.

   (e) What are hazard free circuits?

   (f) What is switching?

   (g) What is the importance of clock in synchronous circuits?

   (h) Why we do machine minimization in digital circuits?

   (i) What is a clock? How can we reduce clock frequency to one fourth? Draw the circuit?

   (j) Flip flop can also be used as latch. Justify the statement. (2×10=20)